Master's Thesis

ULTRA-LOW-JITTER, MMW-BAND FREQUENCY SYNTHESIZERS BASED ON A CASCADED ARCHITECTURE

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ABSTRACT

This thesis presents an ultra-low-jitter, mmW-band frequency synthesizers based on a cascaded architecture. First, the mmW-band frequency synthesizer based on a CP PLL is presented. At the first stage, the CP PLL operating at GHz-band frequencies generated low-jitter output signals due to a high-Q VCO. At the second stage, an ILFM operating at mmW-band frequencies has a wide injection bandwidth, so that the jitter performance of the mmW-band output signals is determined by the GHz-range PLL. The proposed ultra-low-jitter, mmW-band frequency synthesizer based on a CP PLL, fabricated in a 65-nm CMOS technology, generated output signals from GHz-band frequencies to mmW-band frequencies, achieving an RMS jitter of 206 fs and an IPN of –31 dBc. The active silicon area and the total power consumption were 0.32 mm^2 and 42 mW, respectively. However, due to a large in-band phase noise contribution of a PFD and a CP in the CP PLL, this first stage was difficult to achieve an ultra-low in-band phase noise. Second, to improve the in-band phase noise further, the mmW-band frequency synthesizer based on a digital SSPLL is presented. At the first stage, the digital SSPLL operating at GHz-band frequencies generated ultra-low-jitter output signals due to its sub-sampling operation and a high-Q GHz VCO. To minimize the quantization noise of the voltage quantizer in the digital SSPLL, this thesis presents an OSVC as a voltage quantizer while a small amount of power was consumed. The proposed ultra-low-jitter, mmW-band frequency synthesizer fabricated in a 65-nm CMOS technology, generated output signals from GHz-band frequencies to mmW-band frequencies, achieving an RMS jitter of 77 fs and an IPN of –40 dBc. The active silicon area and the total power consumption were 0.32 mm^2 and 42 mW, respectively.

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TECHNICAL TERMS AND ABBREVIATIONS

QAM	Quadrature amplitude modulation
5G	Fifth-generation mobile system
IPN	Integrated phase noise
EVM	Error-vector magnitude
RF	Radio frequency
DAC	Digital-to-analog converter
ADC	Analog-to-digital converter
LO	Local oscillation
VCO	Voltage-controlled oscillator
PLL	Phase-locked loop
FoM	Figure of merit
RFD	Reference-frequency doubler
CP	Charge pump
PFD	Phase-frequency detector
DSM	Delta-sigma modulator
LF	Loop filter
ILFM	Injection-locked frequency multiplier
OSVC	Optimally-spaced voltage comparators
SSPLL	Sub-sampling phase-locked loop
DLF	Digital loop filter
FLL	Frequency-locked loop
mmW	Millimeter wave
FTL	Frequency-tracking loop
SH	Sample and hold
QVCO	Quadrature voltage-controlled oscillator
TDC	Time-to-digital converter

1. Introduction

As the demand for both wireline and wireless communication systems with high data rates increases, generating ultra-low-jitter, millimeter-wave-band (mmW-band) signals is more significant in the development of the transceivers. New radio frequencies in mmW bands are defined by the recent fifth-generation (5G) mobile network specification to transmit and receive data across a broader bandwidth [1]. The 5G network must also use high-order modulations to achieve super-high data speeds, such as more than 10 Gb/s. The level of the error-vector magnitude (EVM) must be reduced to support QAM, which means that mmW-band LO signals require ultra-low IPN [2]. Likewise, direct RF-data converters based on high-speed ADCs also must have output signals in mmW-bands with ultra-low RMS jitter [3], to satisfy the Nyquist criterion and reduce the effect of channel mixing. In advanced high-speed serial links, recent demands on ultra-low jitter performance for mmW-band output signals also increase, where target data rates are higher than 100 Gb/s [4].

Accordingly, in many different advanced applications, mmW-band output signals are used, but the ultra-low RMS jitter is commonly expected. A CP PLL achieving an extremely low RMS jitter at 14 GHz was presented [3]. However, it must use a reference clock with a very high frequency, i.e. 500 MHz, to reduce the in-band phase noise. Capable solutions for generating ultra-low-jitter signals are a SSPLL [5] and an ILFM [6]. However, when mmW-band output signals are generated directly based on a single-stage architecture, both single-stage frequency synthesizers have issues with stable operation, which will be discussed in detail in Chapter 2. In this thesis, mmW-band frequency synthesizers based on a cascaded architecture generating ultra-low-jitter, mmW-band output signals were presented [7], [8]. First, the proposed mmW-band frequency synthesizer based on a CP PLL uses a high figure-of-merit (FoM) GHz-range PLL combination with low-jitter injection-locked frequency multipliers (ILFMs). As a result, the output signals at mmW-band from the proposed frequency synthesizer can achieve an ultra-low IPN satisfying the specifications of 5G systems. However, since the overall jitter performance of the cascaded architecture fully depends on the performance of the first stage GHz-range PLL (discussed in Chapter 3), the in-band phase noise is restricted by the PFD and CP in the CP PLL.

Second, the proposed mmW-band frequency synthesizer based on a digital SSPLL was presented. The SSPLL operates at relatively low frequencies at the first stage so that low out-band phase noise and a wide lock-in range can be achieved. The design of the digital PLL has become general since it can overcome the conventional issues of analog design, such as the variation in jitter performance caused by variations in process-voltage-temperature (PVT) [9], [10] and a large silicon area [10], [11]. This trend also motivated the implementation of digital SSPLLs using ADCs for the digitalization of the sampled voltage, thereby quantizing phase errors [12]–[14]. However, to minimize the quantization

noise that limits the level to which jitter can be lowered is challenging for these digital SSPLLs. Digital PLLs require high-performance ADCs to reduce the quantization noise, which simultaneously have high sampling frequencies, fine resolutions, and full-scale input voltage signal coverage, but they necessitate more power consumption and a larger silicon area inevitably. To solve this dilemma of the quantization noise issue throughout traditional digital SSPLLs, a new quantization technique in the voltage domain is presented using the proposed OSVC which only requires a small amount of silicon area and power, while minimizing the quantization error. This thesis is organized as follows. Chapter 2 provides the practical problems of single-stage architectures. The design of the mmW-band frequency synthesizer based on a CP PLL and the limitation of CP PLL are presented in Chapter 3. In Chapter 4, the design of the mmW-band frequency synthesizer based on a digital SSPLL is presented. The experimental results and the conclusions are presented in Chapter 5 and 6, respectively.

2. Practical problems of single-stage frequency synthesizers

2.1. Single-stage ILFMs

An ILFM is promising solution for achieving ultra-low jitter. However, this architecture suffers from severe operational issues when mmW-band output signals are generated directly based on a single-stage architecture. Despite the great performance of reducing a VCO's phase noise, when the multiplication factor, N, is excessively increased to generate a high output frequency, f_{OUT}, an ILFM cannot guarantee reliable operation. A simulation with a conventional mmW-band ILFM [16] was done to address this problem. The output frequency of the mmW-band ILFM's free-running VCO was 28.5 GHz. The power consumption, the quality factor, and the tuning range were 5 mW, 9, and 10%, respectively. The level of the red dotted line of Fig. 1 indicates the max frequency drift, f_{DR}, of the free-running VCO of the ILFM due to temperature variations between –30 and 120 °C. Due to the very high VCO frequency, f_{VCO}, of 28.5 GHz, the large ratio of PVT-sensitive parasitic capacitances results in a large increase in f_{DR}, which was 228 MHz in this simulation. In Fig. 1, the blue solid line indicates the decrease of the same ILFM's lock range, f_L, changing the reference frequency, f_{REF}, from 5.7 GHz to 100 MHz. As N increased, the effective current of the Nth harmonic component of the injection signal reduced regarding the core current of the VCO, thus decreasing the injection strength and f_L [17]. When N exceeded 12, f_L dropped below the maximum f_{DR}. Thus, the ILFM requires an additional frequency-tracking loop (FTL) correcting the f_{DR} of the VCO in the background. When N reached to 285 and f_{REF} was 100 MHz, f_L was decreased to 18 MHz. For the ILFM's stable operation, the FTL's resolution and precision must be very high in these extreme cases, but in practice designing such an FTL is very challenging.

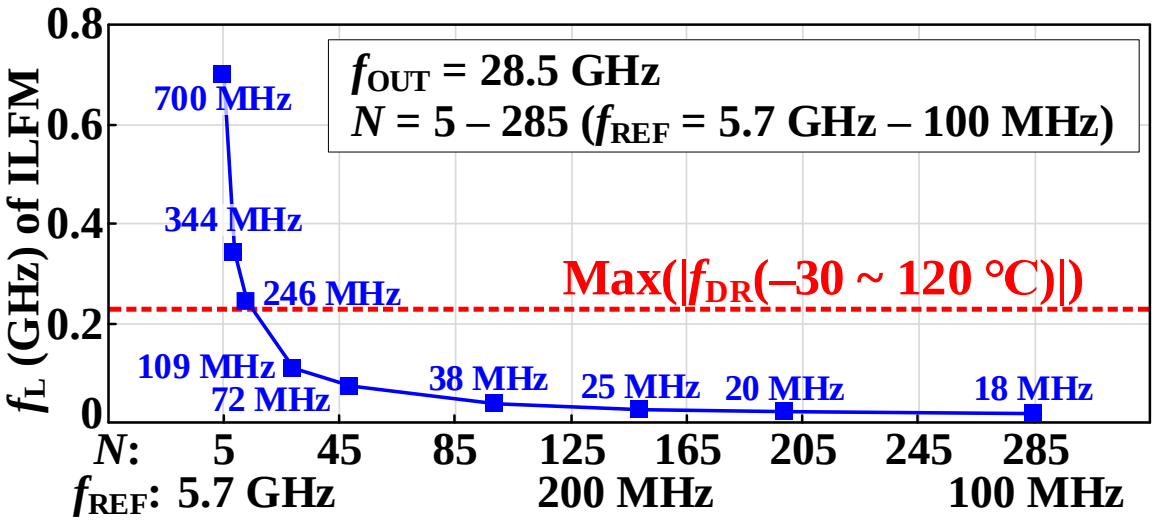


Figure 1. The change of f_L of a single-stage ILFM with the maximum f_{DR} of a free-running VCO.

2.2. Single-stage SSPLLs

Another possible solution for the generation of ultra-low-jitter signals is an SSPLL. However, when mmW-band output signals are generated, a direct mmW SSPLL is also not reliable due to the small lock-in range, f_{LI}. The change of f_{LI} of a single-stage, mmW-band SSPLL is shown in Fig. 2, changing f_{REF} from 5.7 GHz to 100 MHz. The simulation was done using the same VCO in mmW-bands, and f_{LI} was defined as the maximum instantaneous disturbance at which the SSPLL can cover f_{VCO} to the target frequency without the false-locking problem [18]. Thus, when f_{LI} is small, the operation of the SSPLL is susceptible to the variations in f_{VCO}. At every reference period ($1/f_{REF}$), SSPLLs monitored the disturbance in f_{VCO}, so when N is small, they can detect and correct it frequently. However, the period of the detecting and correcting the frequency error becomes slower as N increases, which reduces f_{LI}. As N increased, f_{LI} decreased dramatically as shown in Fig. 2, and when N was 285, f_{LI} was a very small value of 19 MHz. For this issue, SSPLLs must use large power due to a use of an additional FLL operating at mmW-band frequencies. Additionally, since direct mmW-band SSPLLs' phase-noise skirt is determined by the VCO operating at a mmW-band frequency, there is a limitation of reducing the out-band phase noise. When a VCO oscillates in mmW bands, it has a relatively low-quality factor since the quality factor of the capacitive components of the *LC* tank decreases significantly [19] – [22].

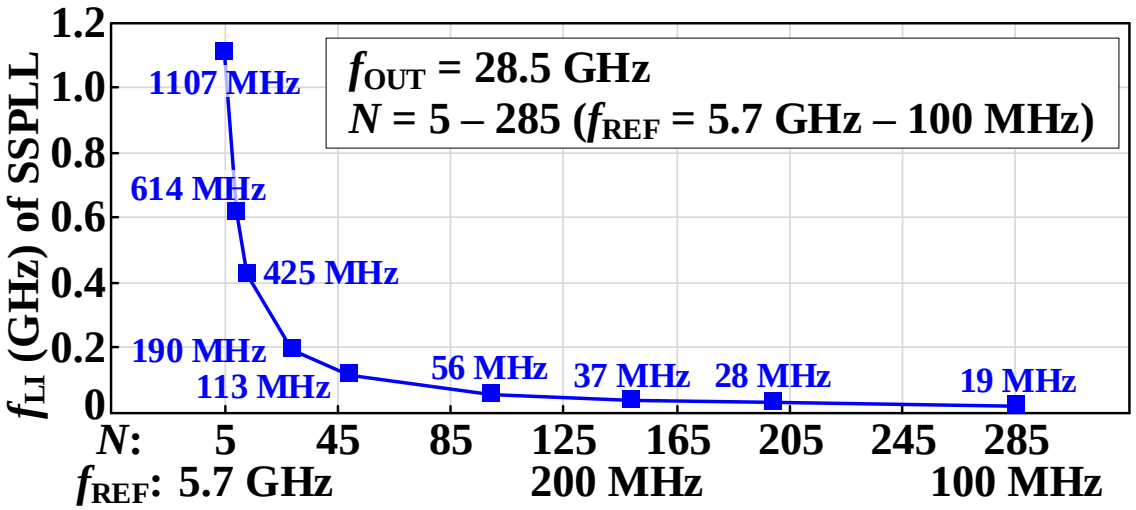


Figure 2. The change of f_{LI} of a single-stage SSPLL.

3. Design of the mmW-band frequency synthesizer based on a CP PLL

3.1. Concept

The conceptual architecture and the conceptual phase noise of the mmW-band frequency synthesizers based on a CP PLL are shown in Figs. 3 and 4, respectively. In this thesis, 120-MHz f_{REF} of the reference signal, S_{REF}, was used. At the first stage, a CP PLL generates the GHz-range signal, S_{CPPLL}, having the frequency, f_{CPPLL} as shown in Fig. 3. For the proper first-stage multiplication factor, N_1, f_{CPPLL} can be selected to be at specific frequencies, where the VCO's phase-noise performance is the best. Thus, f_{CPPLL} was around 3 to 4 GHz when the values of N_1 were controlled around 20 to 40. Due to a GHz-range VCO having a high-quality factor, S_{CPPLL} can achieve low out-band phase noise, which is represented by the blue line in Fig. 4. By multiplying f_{CPPLL} by N_2 times, where N_2 is the second-stage multiplication factor, an ILFM generates the mmW-band signal, S_{OUT}, having the frequency, f_{OUT}, at the second stage. For this frequency multiplication, an ILFM is a viable solution. First, the ILFM does not have external building block that can worsen S_{OUT}'s in-band phase noise. Second, the ILFM can reduce the phase noise of the mmW-band VCO sufficiently due to the sufficiently extended bandwidth. Therefore, as shown in the red line in Fig. 4, S_{OUT}'s phase noise can follow S_{CPPLL}'s phase noise up to a very high frequency offset with the theoretical value of $20\log(N_2)$, which means that, there would be no degradation in the RMS jitter from S_{CPPLL} to S_{OUT} theoretically.

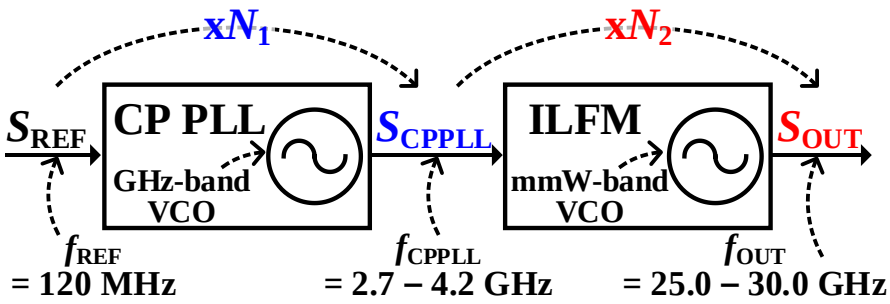


Figure 3. Conceptual architecture.

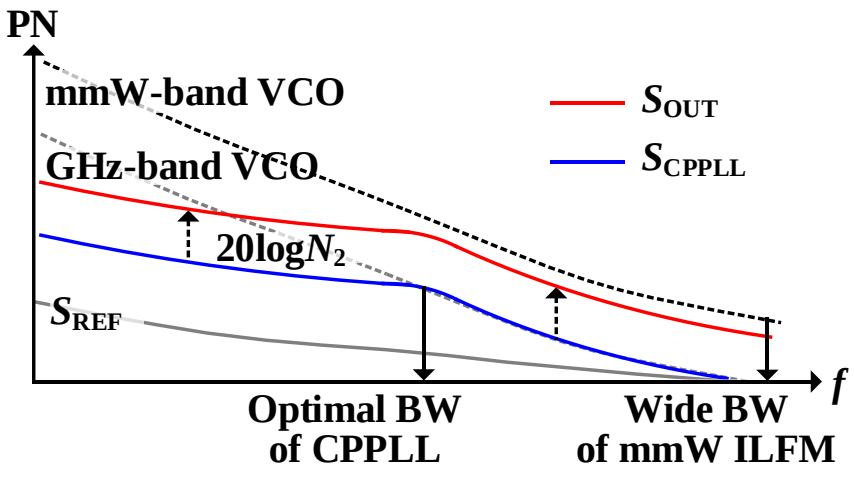


Figure 4. Conceptual phase noise.

3.2. Advantages

For applications that must cover multiple bands over a wide spectrum, this frequency synthesizer based on a cascaded architecture also has additional advantages. First, it can save power consumption when low-frequency signals are generated. If a single-stage, mmW-band frequency synthesizer was used, it would require subsequent mmW-band-frequency dividers for the generation of low-band signals while consuming additional power. However, since in this cascaded architecture, only the GHz-band PLL at the first stage has to operate, the additional use of power can be avoided. Second, since ILMFs with different N_2s can cover multiple frequency bands, it can easily extend the coverage range. By simply adding ILFMs having proper N_2s, it is easy to add new frequency bands to the existing frequency plan. Even though a lot of ILFMs are required to cover different bands, any frequency drifts of the ILFMs can be corrected by a single FTL [7], which prevents the phase-noise degradation of all signals in multiple bands. Finally, in a transceiver, multiple signals for multiple channels far apart each other can be distributed by this cascaded architecture with efficient power. It is possible to save the power consumption of the signal distributions by transmitting a first-stage signal of the GHz-band PLL to all channels globally, and then providing a signal locally using an mmW-band ILFM in each channel. This architecture also can reduce the imbalance of the quadrature signals, since the ILFM can generate the quadrature signals right in front of each channel.

3.3. Implementation

3.3.1. Fractional-*N* CP PLL

Figure 5 shows the overall architecture of the fractional-*N* CP PLL. Low-IPN signals from 3 to 4 GHz are generated using the $2f_{REF}$-reference clock signal, S_{RFD}, from the preceding reference-frequency doubler (RFD). The CP PLL is implemented as a conventional type-II PLL architecture using a delta-sigma modulator (DSM) based on a 1-2 MASH structure. Due to the doubled reference frequency, the division number of the divider can be halved, which can suppress the degradation in the in-band noise by building blocks, such as a PFD, a CP, and a divider. Additionally, since the DSM's operating frequency is doubled, the DSM's quantization noise can be suppressed naturally. In the passive loop filter of the CP PLL, the characteristics are determined mainly by $C1$, $C2$, and $R2$. In the layout, an additional RC-RC filter was placed right in front of the control voltage node of the VCO to suppress high-frequency noise through the long metal line from the loop filter to the control voltage. This RC-RC filter, consisting of $R3$, $C3$, $R4$, and $C4$, also provides an additional filtering to suppress the reference spur and the DSM's quantization noise and can be used to calibrate the phase margin of the loop.

3.3.2. mmW-band ILFM

Figure 6 shows the schematics of the mmW ILFM. To generate the quadrature signal, the differential outputs of the CP PLL was used at the divide-by-2 divider. The quadrature injection signals (*INJ*_I±/Q±) is generated by the pulse generators (PGs) and delivered to the quadrature VCO (QVCO) in mmW-band. An FTL was used for the calibration of frequency drifts of the QVCO, while consuming less than 900 μW [16].

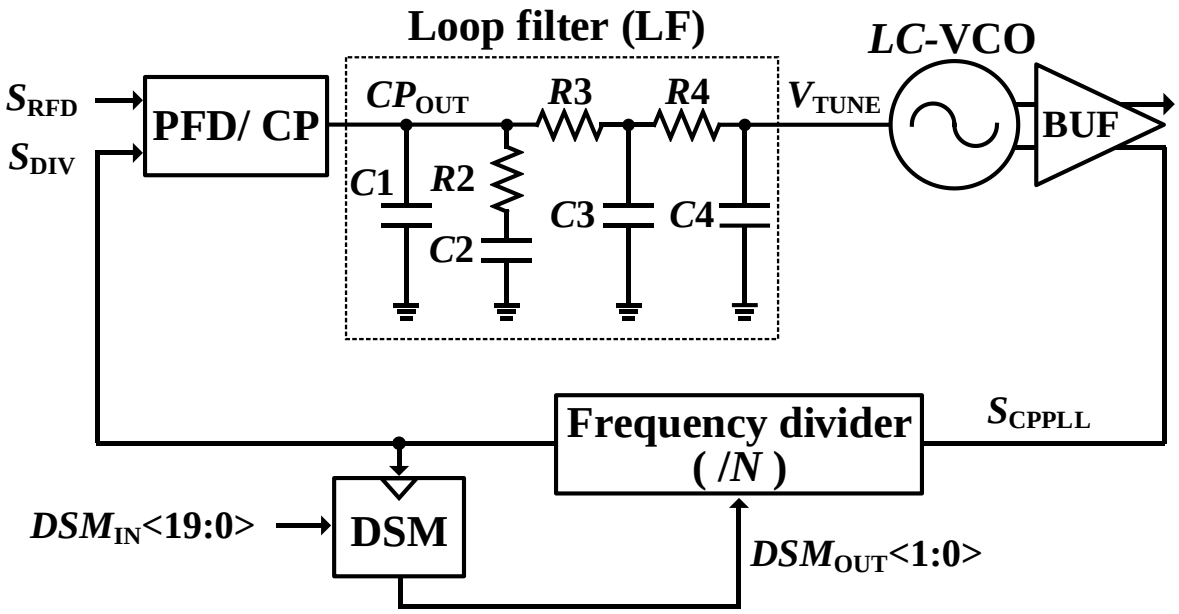


Figure 5. Schematics of Fractional-*N* CP PLL.

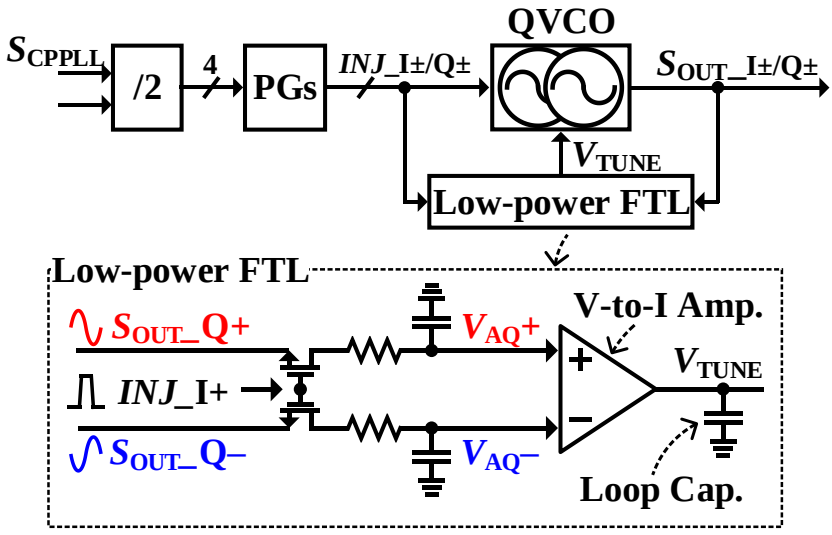


Figure 6. Schematics of mmW-band ILFM.

3.2. Limitation of the CP PLL

Since the additional jitter from the ILFM can be reduced to a negligible level, designing a GHz-band CP PLL having ultra-low jitter is the most critical to generate mmW-band signals that have ultra-low output jitter. However, CP PLL has a limitation of reducing the phase noises of the PLL's components, such as, PFD and CP which are dominant components in general. To reduce this in-band noise further, SSPLL can be a good solution. Unlike the CP PLL, SSPLL can have an ultra-low in-band phase noise due to the high detection gain of a subsampling PD (SSPD). Also, since it can achieve a sufficiently wider lock-in range than a single-stage, mmW-band SSPLL, a stable operation can be ensured in this GHz-band SSPLL. The design of the proposed GHz-band SSPLL is discussed in detail in Chapter 4.

4. Design of the mmW-band frequency synthesizer based on a digital SSPLL

4.1. Conventional digital SSPLLs using a multi-bit ADC

It was very critical to solve the problem of the quantization noise that is a general issue in the digitalization of the PLL, since the target of this thesis was a generation of ultra-low-jitter signals with a digital PLL. In the digital PLL, the precision of the phase-error detection and the correction determines the amount of the quantization noise. Hence, in case that VCO's resolution is high enough, the amount of the quantization noise mainly depends on the precision of a voltage quantizer which converts the sampled analog voltage to digital value including the phase-error information. The conceptual architecture of a conventional digital SSPLL based on an M-bit ADC as a voltage quantizer is shown in Fig. 7, where M is the resolution bit of the ADC. The sampled analog voltage, V_{SH}, from the sample and hold (SH) circuit can be quantified by the M-bit ADC having a $V_{FS}/2^M$-voltage resolution, where V_{FS} is the ADC's full input range. Multiplying the ADC's digital output, D_{VC}, by the error correction gain of the PLL, K, the digital loop filter (DLF) transfers this product of K·DVC to the control voltage, which adjusts the VCO frequency. Generally, the limitation of the in-band phase noise is determined by the quantization error. Since the quantization error is reduced as the voltage resolution of $V_{FS}/2^M$ is more precise, the quantization error can be reduced more by increasing M [14].

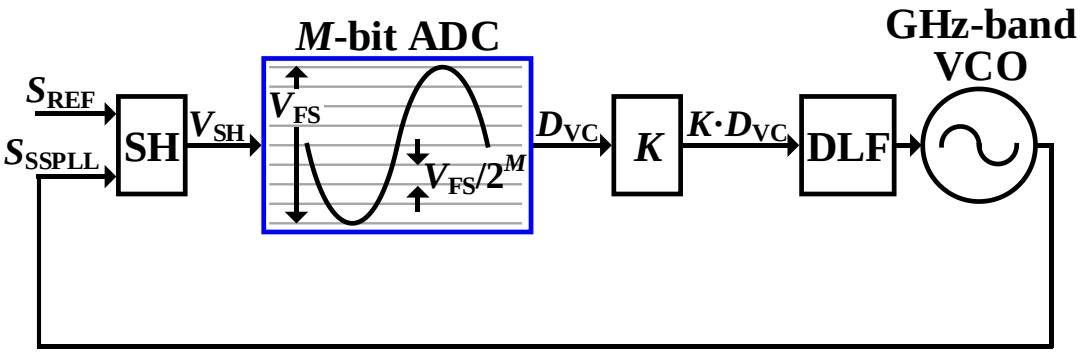


Figure 7. Conceptual architecture of a multi-bit ADC-based SSPLL.

To reduce quantization noise, an eight-bit and a six-bit ADC are used for the digital SSPLLs in [13] and [12], respectively. Likewise, to increase the effective resolution to eight-bit, a preamplifier and a following four-bit ADC were used in [14]. However, the intrinsic trade-off between the level of the quantization error and the value of M exists inevitably. Thus, to achieve an extremely low amount of the quantization noise, an eight-bit ADC must be required at least. However, in practical, achieving such a high resolution is difficult. Even if designing a high-resolution ADC is possible, it must consume a much larger power and require a much larger silicon area. For reducing the quantization noise, there is

another possible solution using a one-bit voltage comparator (VC) instead of the *M*-bit ADC. By observing the output of the one-bit VC, *K* is optimized in the background. This method is already general for the design of BBPD-based digital PLL in the time domain [23], [24] since this can save power consumption and require a smaller area. However, since the one-bit VC can obtain only the binary information which is too small for phase errors, it has a limitation of minimizing the amount of the quantization noise.

4.2. The proposed digital SSPLL using the OSVC

As mentioned above, the main reason for the limitation of the digital SSPLL is that phase-error information from a one-bit VC is too small. Hence, by increasing the numbers of decision thresholds and representative levels with the order of the optimization, this limitation can be solved theoretically. This method was first applied in [25] to minimize the quantization error of a time-domain digital PLL. This digital PLL with three BBPDs can minimize the quantization noise sufficiently optimizing *K* and the spacings between the time thresholds of the BBPDs. We found that this concept of the quantization noise reduction of the BBPD-based digital PLL could also be implemented in the voltage-domain SSPLL, thus an OSVC-based digital SSPLL was presented [8].

Figure 8 shows the conceptual architecture of the OSVC-based digital SSPLL. The proposed OSVC consists of three one-bit VCs having different threshold voltages, V_{TH}s. An SH circuit samples the voltage level of the output signal, S_{SSPLL}, of the SSPLL as V_{SH}. Then, the OSVC quantizes the voltage error, v_{ERR}, between V_{SH} and the reference voltage, V_{REF}, which includes the phase-error information. The OSVC has an optimal spacing between the V_{TH}s of the one-bit VCs by optimizing V_{TH}s. Even though V_{TH}s have equal spacing theoretically, in practice, each V_{TH} requires individual controller due to nonidealities in the OSVC, such as mismatches and input offsets, V_{OS}s. Hence, when the number of V_{TH}s increases, the OSVC requires increased design complexity. Simulations selecting the number of V_{TH}s were performed in Simulink by estimating the PLL jitter as the number of V_{TH}s is changed. In these simulations, as the number of V_{TH}s increased, the PLL jitter was improved gradually, but the ratio of improvement became small. The PLL jitter was improved by 16%, when the number of V_{TH}s increased from one to three, but the improvement was only 4% and 1%, when the number of V_{TH}s increased from three to five and from five to seven, respectively. Considering the fundamental trade-off between the performance of the PLL jitter and the design complexity, the number of V_{TH}s was set at three in this digital SSPLL. As shown in Fig. 8, three VCs with three different decision thresholds, i.e., 0, and $\pm V_{TH}$, quantize V_{SH}.

Figure 9 shows the probability-density function (PDF) of v_{ERR} with four representative levels, i.e., $\pm K$, and $\pm 3K$. By co-optimizing the spacing of V_{TH}s and the value of K, the amount of the quantization noise can be minimized significantly by the OSVC with low power and low complexity. This method is much more attractive in the voltage domain than in the time domain [25] since the OSVC can use delta-sigma DACs (ΔΣDACs) for the accurate calibration of V_{TH}. To optimize V_{TH}s and K to the optimal values that can minimize the variance of v_{ERR}, the Lloyd-Max algorithm in [26] was used. This algorithm can provide the proper solution for decision thresholds and the representative levels, which can reduce the variance of the quantization error of any PDFs. From this algorithm, the optimal spacing of V_{TH}s and the value of K are obtained as σ_{ERR} and $0.5\sigma_{ERR}$, respectively, where σ_{ERR} is the standard deviation of v_{ERR}. The reason of these simple solutions is that the PDF of v_{ERR} follows Gaussian distribution [27]. These solutions are used to control the spacing of V_{TH}s by the V_{TH}-controller, which is discussed in detail in Chapter 4.4.2.

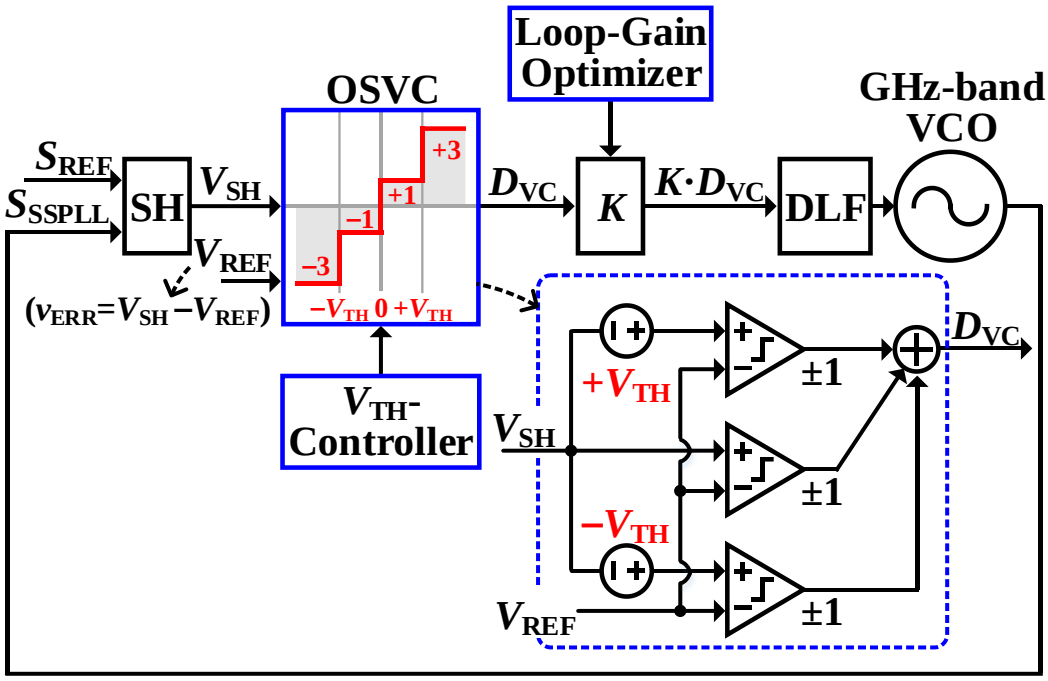


Figure 8. Conceptual architecture of an OSVC-based SSPLL.

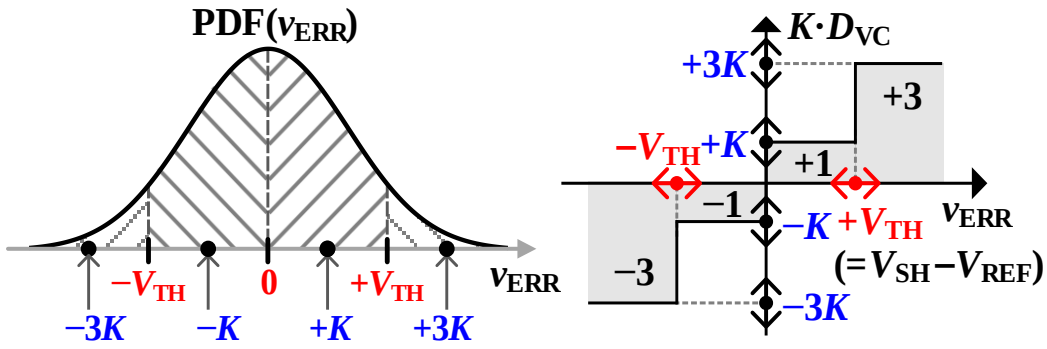


Figure 9. PDF of v_{ERR} with four representative levels.

4.3. The RMS jitters of the multi-bit ADC-based SSPLL and the OSVC-based SSPLL

To estimate how the proposed OSVC can reduce the quantization error effectively, simulations in Simulink was done. In this simulation, the RMS jitter of the typical digital SSPLL using the *M*-bit ADC in Fig. 7 and the proposed digital SSPLL using the OSVC in Fig. 8 were simulated and compared. From this, the value of M that the digital SSPLL using the ADC requires for the same performance of the RMS jitter as the digital SSPLL using the OSVC is evaluated. The simulation setup was that the VCO's period jitter was assumed as 10 fs, and the output jitter of the reference signal of 100 MHz was assumed as 60 fs. To compare the results fairly, the value of K in the digital SSPLL using *M*-bit ADC was fixed as the optimal value according to *M*, which minimizes the SSPLL's RMS jitter. Then, for the two SSPLLs conditions, such as the equal values of 100-MHz f_{REF} and 5-GHz f_{SSPLL} were applied, where f_{SSPLL} is the output frequency of the SSPLL.

As shown in Fig. 10, simulation results show the black and the blue lines, representing the RMS jitters of the digital SSPLL using *M*-bit ADC and the digital SSPLL using the proposed OSVC, respectively. The RMS jitters of the digital SSPLLs are represented in the y-axis, which is a normalized value to that of an ideal SSPLL where there is no quantization noise in the phase detection. The normalized RMS jitter of the digital SSPLL using the OSVC was about 1.06, which implies that the degradation was 6% compared with the ideal SSPLL without the quantization noise. Since the resolution was not fine sufficiently to quantify the quantization noise in the ADC, the RMS jitter of the digital SSPLL using the *M*-bit ADC was almost unchanged until the value of *M* changed from two to six. As the value of *M* was changed from six to nine, the RMS jitter of the SSPLL was reduced gradually, since the ADC could quantize the quantization noise more precisely. Then, when the value of *M* was larger than nine, the RMS jitter was almost unchanged again due to the sufficient resolution of the ADC. Additionally, in Fig. 10, the value of *M* at a crossing point of the black and blue lines is near eight, which implies that typical SSPLLs using the ADC must have an eight-bit ADC to achieve the similar RMS jitter as that of SSPLLs using the OSVC. Since the OSVC can optimize the spacing of the V_{TH}s in the background for a given condition, using the proposed OSVC can significantly reduce the burden of the *M*-bit ADC in the digital SSPLL where a high value of *M* is required for suppressing the quantization noise sufficiently. Thus, the digital PLL using the proposed OSVC can achieve low jitter performance more efficiently while consuming low power and requiring a small area.

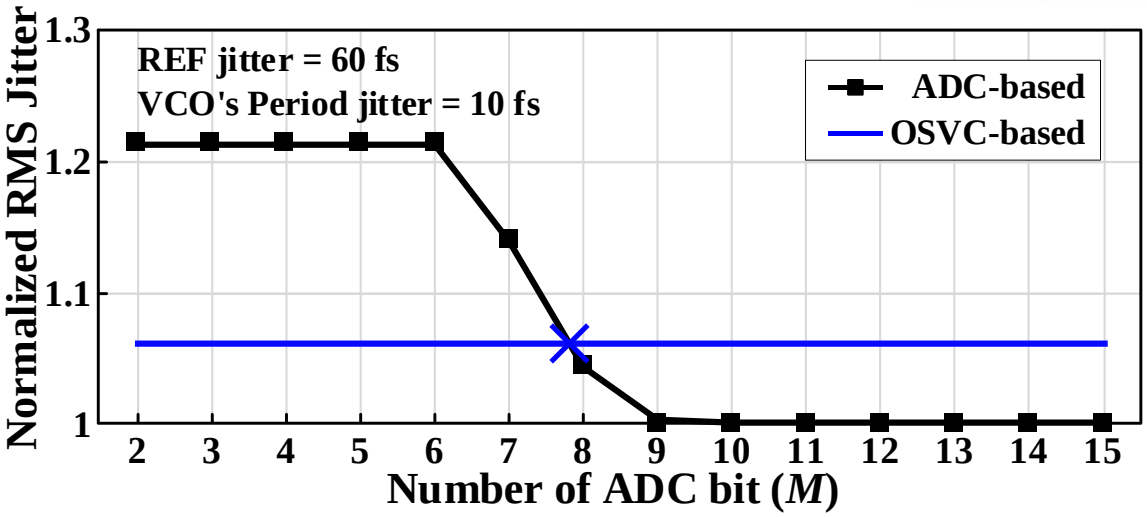


Figure 10. The normalized RMS jitters of the SSPLLs using the M-bit ADC and the OSVC.

4.4. Implementation

4.4.1. Cascaded Architecture

Figure 11 shows the overall architecture of the mmW-band frequency synthesizer using an OSVC-based GHz-band SSPLL and a mmW-band ILFM at the first stage and the second stage, respectively. The input frequency is multiplied from the mmW-band ILFM by a factor of 15, however, the real N_2 becomes 7.5 since a divide-by-2 divider is included generating quadrature injection signals [7]. Based on a type-II architecture, the SSPLL consists of a differential SH, an OSVC, a digital loop filter (DLF), an LC VCO, and a VCO buffer between VCO and the differential SH circuit. The difference between the differentially-sampled voltages, i.e., $V_{SH,P}$ and $V_{SH,N}$, is detected by the three VCs, i.e., VC_H, VC_M, and VC_L, thereby generating D_H, D_M, and D_L, respectively. By adding the two offset voltages, i.e., V_{TH+} and V_{TH-}, that are generated by the V_{TH}-generator of the OSVC, to the positive input of VC_H and to the negative input of VC_L, the OSVC generates four decision values in the digital output, D_{VC}. According to the analysis in Chapter 4.2, theoretically, the spacings of $+V_{TH}$ and $-V_{TH}$ from 0 are the same. In that case, only one additional threshold voltage of V_{TH} should be generated by the V_{TH}-generator. However, in practice, the VCs have mismatches, which cause intrinsic input offset voltages. The VTH-generator was implemented to generate V_{TH+} and V_{TH-} individually by using two capacitors, i.e., C_{TH+} and C_{TH-}, before the inputs of VC_H and VC_L, respectively, so that even in the presence of these mismatches, the V_{TH}-controller can optimize the two spacings of the threshold voltages. The design of the V_{TH}-generator and the ability of the V_{TH}-controller to compensate mismatches between the VCs are discussed in Chapter 4.4.2.

The DLF consists of the proportional path gain, K_P, and the integral (I) path gain, K_I. To prevent the VCO from the subsampling operation, a buffer was used after the VCO. The source-follower buffer was used in the general SSPLLs [14], [28] to preserve the VCO's sine wave. The buffer can generate sufficiently high output swing due to thick-oxide transistors, resulting in a high gain of the following SH circuit. This high gain can help the SSPLL to have a low in-band phase noise. The V_{TH}s in the OSVC and K_P in the DLF is calibrated in the background by the V_{TH}-controller and the loop-gain optimizer, respectively. The frequency acquisition of the SSPLL was done initially by controlling the VCO frequency manually. To prevent the false-locking issue of the SSPLL, a simple FLL can be used in the background [5].

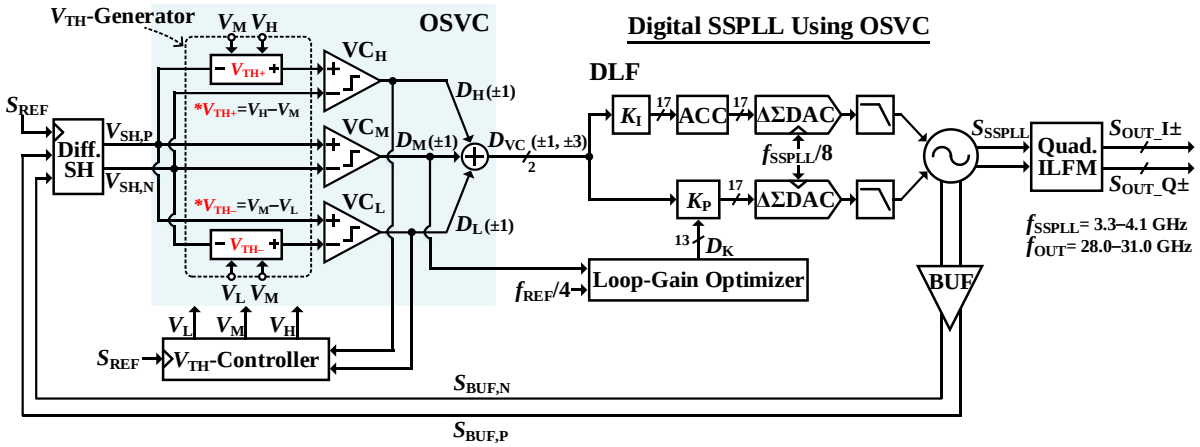


Figure 11. Overall architecture.

4.4.2. OSVC and V_{TH}-controller

Figure 12 shows the schematics of the OSVC with the differential SH circuits. The OSVC consists of the V_{TH}-generator and the three VCs. To sample the input signals, an switch and a capacitor of 35 fF are used for each of the differential paths of the SH. To suppress the reference spur due to the effect of charge injection, complementary dummy SHs were used [29]. To generate D_{VC}, an adder follows the VCs. Figure 13 shows the operation of the SSPLL, starting with the sampling of $V_{SH,P}$ and $V_{SH,N}$ at the falling edge of S_{REF}. In the *'V_{TH} update'* phase, i.e., Φ_1, the V_{TH}-generator redefines V_{TH+} (or V_{TH-}) by charging C_{TH+} (or C_{TH-}) using the updated V_H and V_M (or V_M and V_L). In the next phase, i.e., Φ_2, the connections of C_{TH+} (or C_{TH-}) return to $V_{SH,P}$ (or $V_{SH,N}$) and VC_H (or VC_L), thereby adding V_{TH+} (or V_{TH-}) to the input of VC_H (or VC_L). Then, D_{VC} is generated by the three VCs at the rising edge of Φ_3. To minimize the charge-sharing effect due to the parasitic capacitance, the switches and the input transistors in the V_{TH}-generator were designed to minimal sizes so that the gain reduction of the SH circuit is prevented.

Figure 14 shows the schematics of the V_{TH}-controller. Since there are intrinsic offsets in the VCs, the V_{TH}-generator must control V_{TH+} and V_{TH-} individually to optimize the two V_{TH}s accurately. Hence, V_H, V_M, and V_L are provided by the V_{TH}-controller. Every 128 periods of S_{REF}, the values of V_H and V_L are controlled by the V_{TH}-controller by comparing the accumulation numbers of D_H and D_L with the optimum numbers, N_{TH+} and N_{TH-}, respectively. When the PDF of v_{ERR} (= $V_{SH,P} - V_{SH,N}$) at the input of the OSVC is Gaussian and V_{TH+} and V_{TH-} have optimal values, the averages of D_H and D_L must be settled as 0.68 and –0.68, respectively. The operating frequency of the V_{TH}-controller was designed as much lower value than that of the loop-gain optimizer to prevent the stability problem which can occur from the two calibrations, i.e., the V_{TH}-controller and the loop-gain optimizer. However, if the operating frequency of V_{TH}-controller was too slow, the overall settling time of the calibration system would be too slow. Considering this fundamental trade-off between the stability problem and the settling time, the operating period of the V_{TH}-controller was fixed as 128 periods of S_{REF}. To control the values of V_H and V_L precisely, a ΔΣDAC with a high bit of 17 and the proceeding RC-RC filter were used. The fixed value of V_M was from the DAC's middle voltage. By using the ΔΣDAC to control the values of V_H and V_L, the effective resolution of the OSVC in the voltage domain was below 1 fs, consuming low power of 200 μW and occupying a small area of 0.01 mm^2. When this concept is implemented in the time domain, the resolution of the OT TDC in [25] was limited to 34 fs.

The VC of the OSVC was implemented based on regenerative comparators with double tail topology [30]. To estimate the V_{OS} of the VC, the Monte-Carlo simulations were performed. In these simulations, the standard deviation of V_{OS} was about 4 mV. Then, to verify the effective alleviation of any effects from the V_{OS} of the VC by separately adjusting V_{TH+} and V_{TH-}, another simulation was performed. At the positive input of VC_H, a V_{OS} of VC_H which is relative to VC_M was inserted intentionally as shown in Fig. 15. In this simulation, the relative value of V_{OS} was $V_{OS,H} - V_{OS,M}$, where $V_{OS,H}$ and $V_{OS,M}$ are the intrinsic offsets of VC_H and VC_M, respectively. Then, transient behaviors of the digital SSPLL using the OSVC was performed by changing the value of ($V_{OS,H} - V_{OS,M}$), and monitoring the result of V_{TH+} to verify that it was controlled properly so that any effects of V_{OS} was removed. To cover larger than $\pm 6\sigma_{OS}$ the range was swept from –30 to 30 mV, since the standard deviation of $V_{OS,H} - V_{OS,M}$ is twice that of V_{OS}. The simulated values of V_{TH+} are represented in the blue line as shown in Fig. 16, which are controlled in the background by the V_{TH}-controller and the V_{TH}-generator. The values of V_{TH+} were adjusted to about 2.5 mV when $V_{OS,H} - V_{OS,M}$ was zero. This value was converged as the accumulated value of D_H became equal to N_{TH+}. Also, this value is almost the same as the theoretical value of 2.5 mV, which is σ_{ERR} in the given conditions. As the value of $V_{OS,H} - V_{OS,M}$ increased, the value of VTH+ decreased linearly to compensate the change as shown in Fig. 16. Thus, the values of V_{TH+} + ($V_{OS,H} - V_{OS,M}$) represented in the red line were unchanged, maintaining the value of 2.5 mV over the entire range. The maximum deviation was only 80 μV in the worst case, which implies that the OSVC

alleviates any mismatch effects. Since the operations in V_{CH} and V_{CL} are the same, this simulation can guarantee the proper operations of the V_{TH}-controller and the V_{TH}-generator. Even if there is the phase offset of the SSPLL by $V_{OS,M}$ of VC_M itself in the steady state, the jitter performance is not degraded by this phase offset.

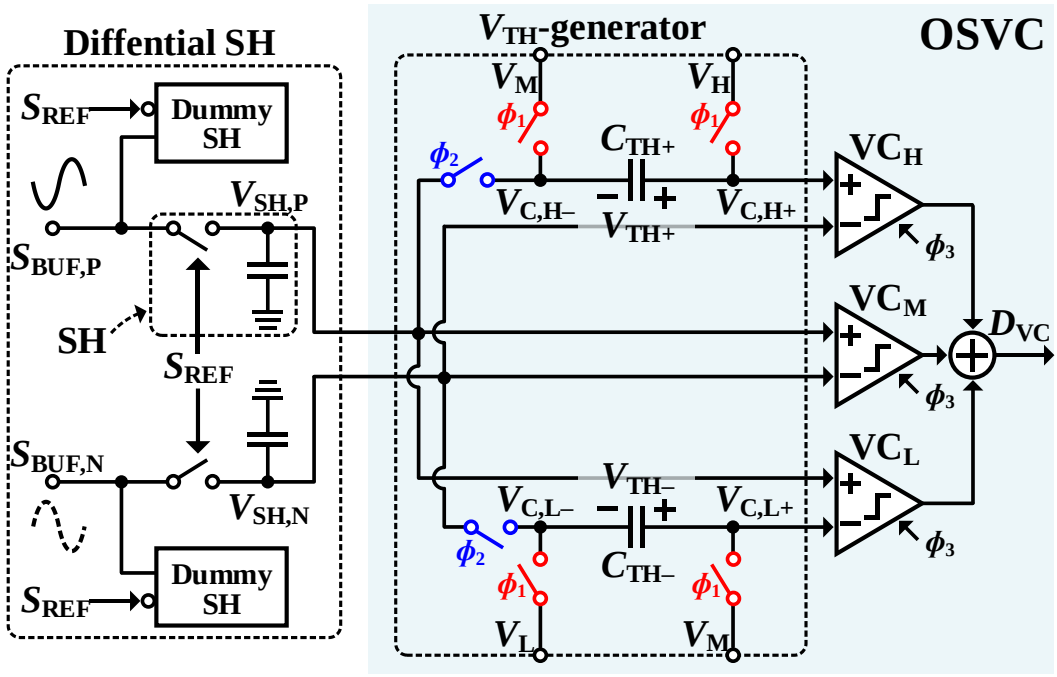


Figure 12. Schematics of the OSVC with Differential SH.

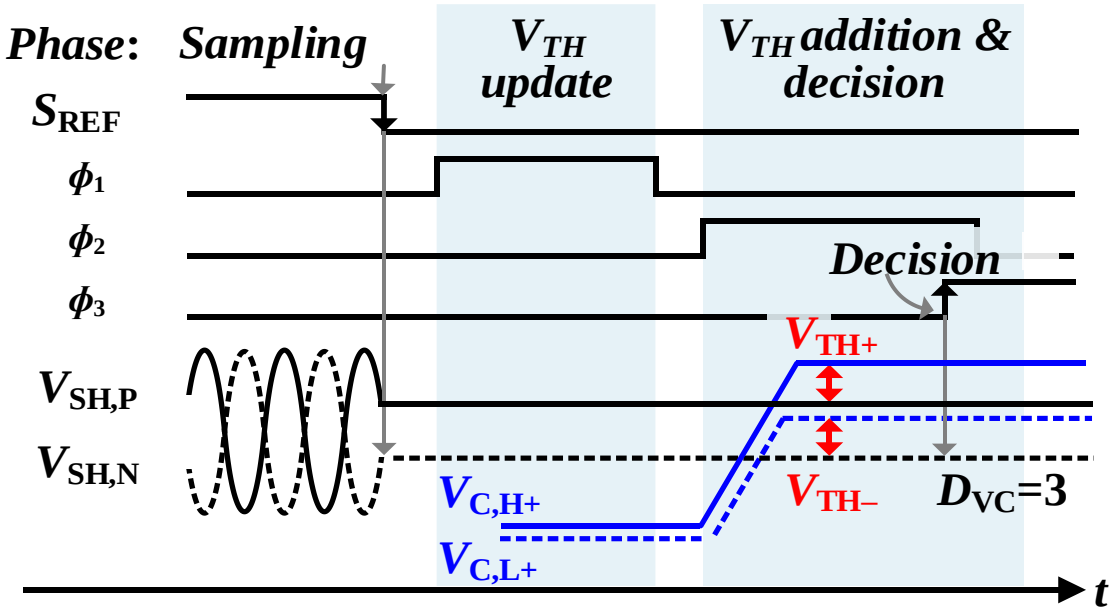


Figure 13. Operation of the OSVC-based SSPLL.

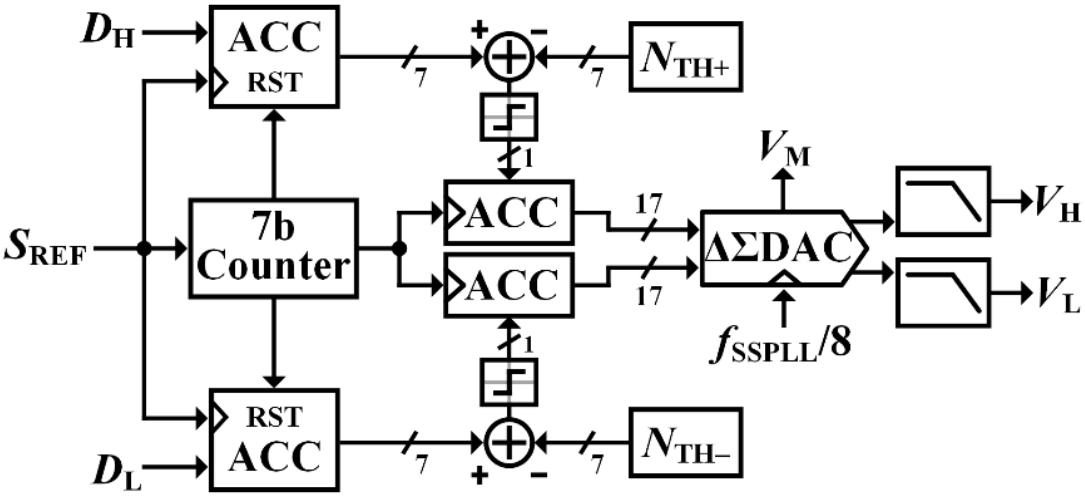


Figure 14. Schematics of the V_{TH}-controller.

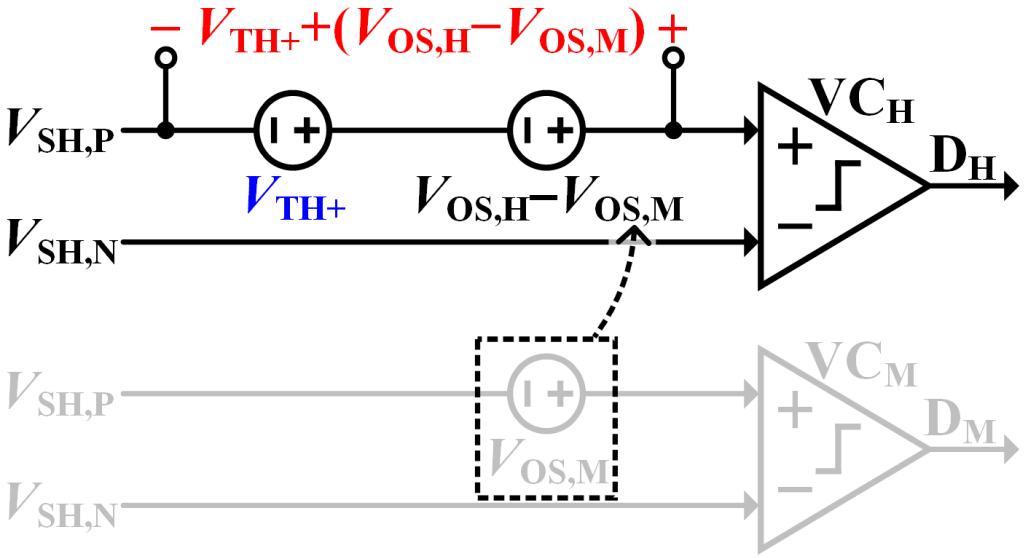


Figure 15. The effective model for the simulation.

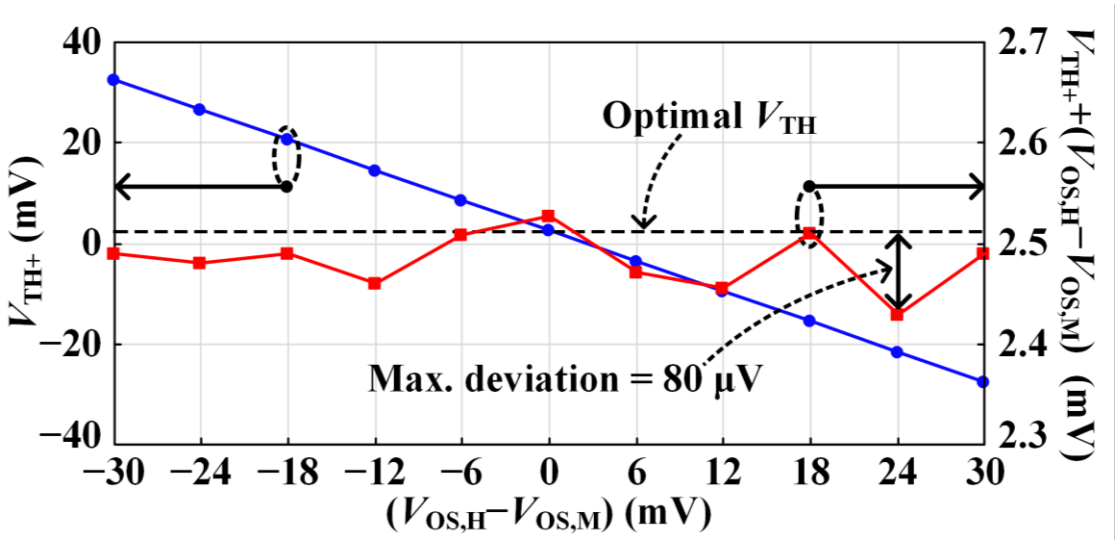


Figure 16. Simulation results.

4.4.3. Loop-gain optimizer

For the design of the loop-gain optimizer, the algorithm in [23] was used. If the value of K_P is too large, the autocorrelation of D_M is minus, since the value of D_M toggles between +1 and –1. On the opposite, if the value of K_P is too small, the autocorrelation of D_M is plus, since the value of D_M is repeated as +1s or –1s. According to the value of the autocorrelation of D_M, the value of K_P is controlled properly. Thus, the loop gain and the bandwidth of the digital SSPLL can be maintained optimal value by controlling the value of K_P in the DLF in the background. To estimate the settling times of the calibration systems, we performed another simulation. At the initial stage, the output of the loop-gain optimizer, D_K, was the maximum value, and the output voltages of the V_{TH}-controller, V_{TH+} and V_{TH-}, was zero. Figure 17 shows that the settling time of the loop-gain optimizer with a faster speed was less than 300 μs. Then, the V_{TH}-controller was settled within 2.5 ms while the loop-gain optimizer controls the value of D_K precisely. As shown in Fig. 18, at the settling moment of DK, the PLL jitter was reduced significantly, and it was improved gradually as the values of V_{TH+} and V_{TH-} was settled to optimum values.

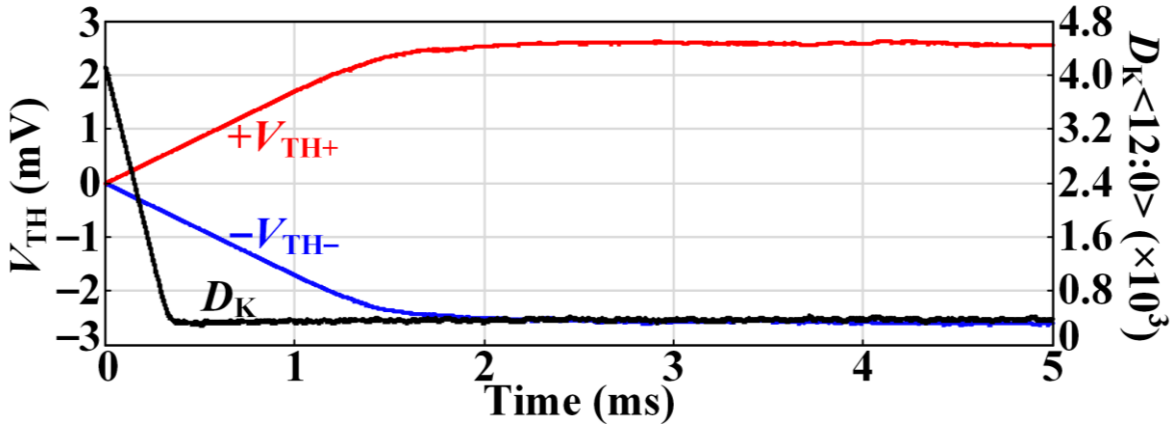


Figure 17. Simulated settling behaviors of the calibration.

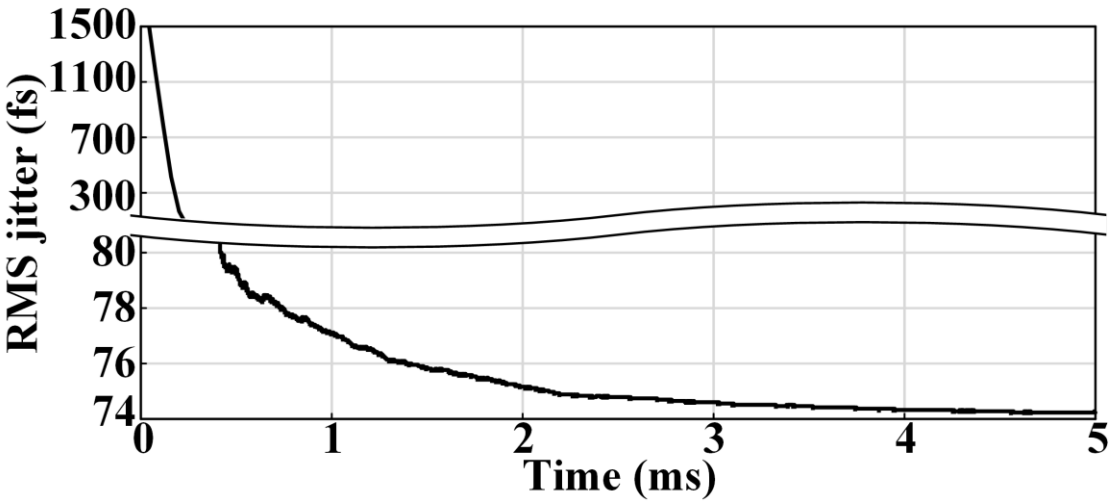
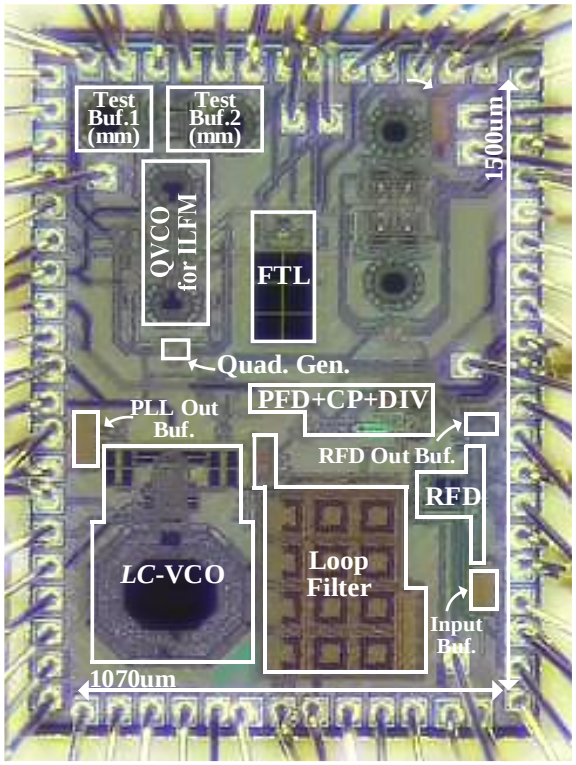


Figure 18. Simulated variation in the RMS jitter.

5. Experimental Results

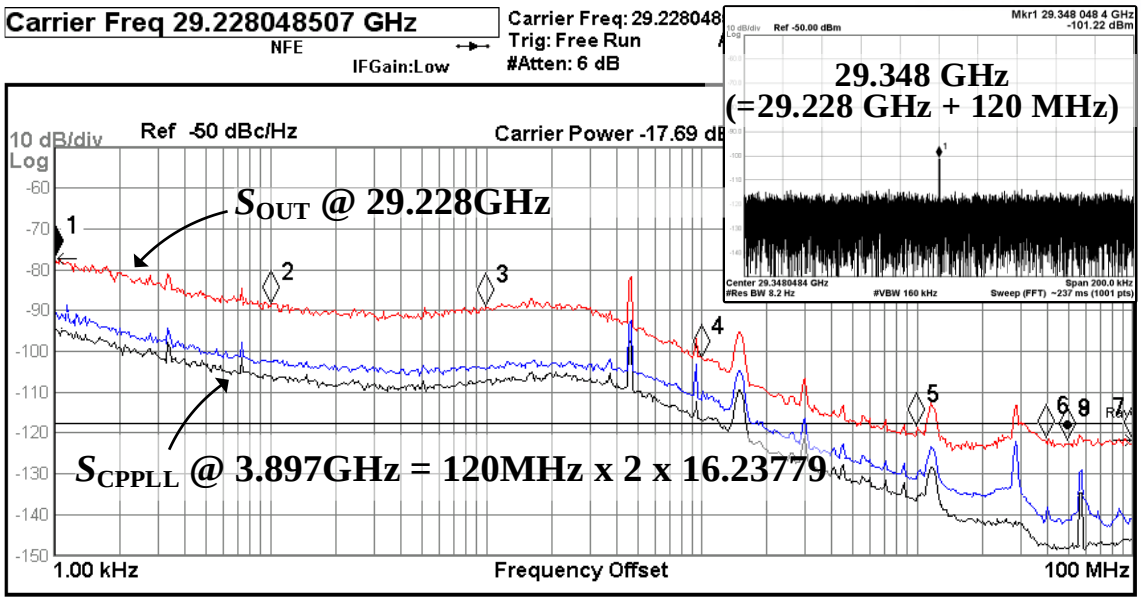
5.1. mmW-band frequency synthesizer based on a CP PLL

The proposed mmW-band frequency synthesizer based on a CP PLL was fabricated in a 65-nm CMOS technology. Figure 19 shows that when the output frequency of the ILFM was 29.22 GHz, the total power consumption was 36 mW. Figure 20 shows the measured phase noises of the output signals of the CP PLL, and the ILFM in the fractional-*N* mode. The measured RMS jitter and IPN at 29.22 GHz were 206 fs and −31 dBc, respectively. Figure 21 shows the measured phase noises of the output signals in the integer-*N* mode. The measured RMS jitter and IPN at 28.8 GHz were 172 fs and −33 dBc, respectively. In Figs. 22 and 23, both measurements show that the level of the 120-MHz reference spur at the mmW-band output was measured as below –83 dBc. Additionally, the phase noise of the ILFM followed the phase noise of the CP PLL with the theoretical value of $20\log(N_2)$, which implies that the added noise from the ILFM was almost negligible.



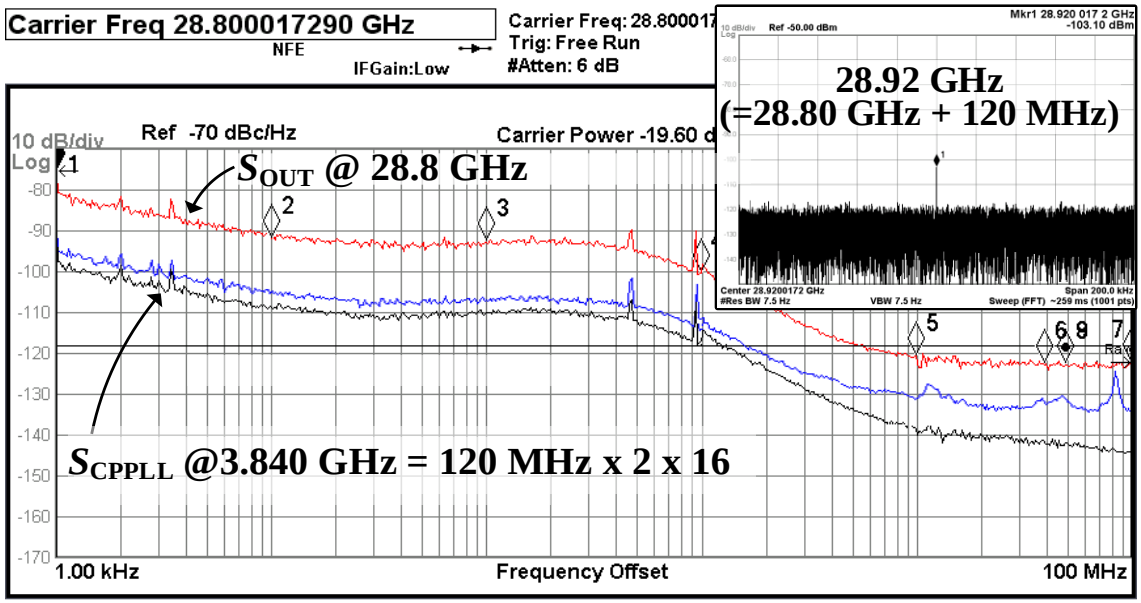
Power Consumption (mW)		
RFD		2.5
CP PLL (20.1)	*LC*-VCO	6.0
	PFD+CP	2.2
	Divider+DSM	3.0
	VCO buf.+Quad. gen.	8.9
ILFM (13.8)	QVCO	10.4
	PGs	2.5
	FTL	0.9
Total	(RFD+PLL+ILFM)	36.4

Figure 19. Die photo and the power breakdown.



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-77.15dBc/Hz			
2	N	2	10.0 kHz	-88.66dBc/Hz			
3	N	2	100 kHz	-89.43dBc/Hz			
4	N	2	1.00 MHz	-101.95dBc/Hz			
5	N	2	10.0 MHz	-118.72dBc/Hz			
6	N	2	40.0 MHz	-121.29dBc/Hz			
7	N	2	100 MHz	-121.82dBc/Hz			
8	N	2	50.0 MHz	-122.24 dBc/Hz	Integ Noise	100 MHz	206.2 fs
9	N	2	50.0 MHz	-122.24 dBc/Hz	Integ Noise	100 MHz	-31.45 dBc

Figure 20. Measured phase noise and spectrum in the fractional-*N* mode.



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	2	1.00 kHz	-75.49dBc/Hz			
2	N	2	10.0 kHz	-91.89dBc/Hz			
3	N	2	100 kHz	-92.75dBc/Hz			
4	N	2	1.00 MHz	-100.33dBc/Hz			
5	N	2	10.0 MHz	-120.69dBc/Hz			
6	N	2	40.0 MHz	-122.68dBc/Hz			
7	N	2	100 MHz	-122.38dBc/Hz			
8	N	2	50.0 MHz	-122.80 dBc/Hz	Integ Noise	100 MHz	172.3 fs
9	N	2	50.0 MHz	-122.80 dBc/Hz	Integ Noise	100 MHz	-33.14 dBc

Figure 21. Measured phase noise and spectrum in the integer-*N* mode.

Table 1 shows the comparison of the performance of the proposed cascaded frequency synthesizer with that of the state-of-the-art fractional-*N* frequency synthesizers in mmW-bands. This work achieved the lowest values of RMS jitter, IPN, and FoM_{JIT} among mmW-band frequency synthesizers.

Table 1. Comparison with the state-of-the-art frequency synthesizers in mmW-bands.

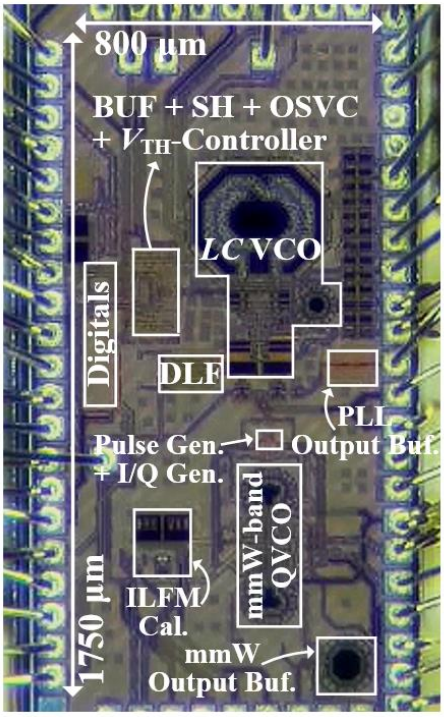
	This work	ISSCC'15	ISSCC'17 [33]	JSSC'14	JSSC'14 [31]
Process	65nm CMOS	32nm SOI	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	RFD + GHz-PLL +ILFMs	Analog/Digital Hybrid PLL	All-Digital PLL	All-Digital PLL	GHz-PLL + ILFM chain
Type	Fractional-*N*	Fractional-*N*	Fractional-*N*	Fractional-*N*	Fractional-*N*
Quadrature	YES	NO	NO	NO	NO
Multi. Freq. Bands	YES	NO	NO	NO	YES
Output Freq. (GHz)	25.0 – 30.0 5.2 – 6.0 2.7 – 4.2	13.1 – 28.0	50.2 – 66.5	56.4 – 63.4	20.6 – 48.2 10.1 – 18.3 3.4 – 6.1
f_{REF} (MHz)	120	104.5	100	100	100
$Jitter_{RMS}$ @f_O (GHz) (Integ. Range)	206fs @29.22 (1k – 100MHz)	1.03ps* @22.25 (10k – 100MHz)	258fs @65.35 (1k – 40MHz)	590fs @61.87 (10k – 10MHz)	1.02ps** @28.5 (10k – 10MHz)
IPN @f_O (GHz) (Integ. Range)	–31.4 @29.22 (1k – 100MHz)	–19.8* @22.25 (10k–100MHz)	–22.5 @65.35 (1k–40MHz)	–15.8 @61.87 (10k–10MHz)	–17.8** @28.5 (10k–10MHz)
IPN (dBc) Norm. to 28GHz (Integ. Range)	–31.8 (1k–100MHz)	–17.8* (10k–100MHz)	–29.9 (1k–40MHz)	–22.7 (10k–10MHz)	–17.9* (10k–10MHz)
In-band noise (dBc/Hz) @f_O (GHz)	–88.6 @29.22	–71.0 @22.25	–78.7 @65.35	–75.0 @61.87	–54.0 @28.5
In-band noise (dBc/Hz) Norm. to 28GHz	–89.0	–69.0	–86.1	–81.9	–54.1
Ref. spur (dBc)	–83.5	NA	NA	–74	–33
Power (P_{DC}) (mW)	36.4 (x15 mode)	31.0	46.0	48.0	148.3
Active Area (mm^2)	0.95	0.24	0.45	0.48	2.09
FoM_{JIT} (dB)***	–238.1	–224.8	–235.1	–227.8	–218.1

* Calculated from the measurement results ** Calculated from the PN graph in Fig. 22(b) of [31]

***$FoM_{JIT}=10\log(\sigma_t^2 \cdot P_{DC})$ (dB)

5.2. mmW-band frequency synthesizer based on a digital SSPLL

The proposed mmW-band frequency synthesizer was fabricated in a 65-nm CMOS technology. As shown in Fig. 22, the active area and the total power consumption were 0.32 mm^2 and 42 mW, respectively, when the 28.5-GHz signals were generated from the reference signal of 100 MHz. The area and the power consumption of the proposed OSVC including the V_{TH}-controller and the V_{TH}-generator were 0.01 mm^2 and 200 μW, respectively. The measured phase noises of the OSVC-based digital SSPLL at 3.8 and 3.9 GHz were shown in Figs. 23 and 24, respectively. The proposed digital SSPLL achieved ultra-low in-band phase noise due to the subsampling operation and the proposed OSVC for the minimization of the quantization noise. Thus, the measured RMS jitter and IPN were 72 fs and −58 dBc, respectively. Due to the operating frequency of ΔΣDAC, i.e., $f_{SSPLL}/8$, the 25-MHz spur and the 12.5-MHz spur were generated as shown in Figs 23 and 24, respectively. Figure 25 shows that the 100-MHz reference spur was −75 dBc. This low level was achieved by using the voltage buffer between the SHs and the VCO and the additional dummy SHs.



Power Consumption (mW)		
SSPLL (19.1)	GHz-band VCO	8.0
	BUF + SH	7.0
	Digital Logics	3.9
	OSVC (w/ V_{TH}-gen. & cont.)	0.2
ILFM (22.7)	Pulse Gen. + I/Q Gen.	11.4
	mmW-Band VCO	10.4
	ILFM Calibrator	0.9
Total		41.8

Figure 22. Die photo and the power breakdown.

The measured RMS jitters of the OSVC-based digital SSPLL, when the output frequency of the SSPLL swept from 3.3 to 4.1 GHz as shown in Fig. 26. The digital SSPLL achieved ultra-low jitter maintaining less than 80 fs across the entire output frequencies. This is because the V_{TH}-controller and the loop-gain optimizer controlled the values of V_{TH}s of the OSVC and K of the loop in the background. Figure 27 shows that the proposed mmW-band frequency synthesizer based on a digital SSPLL achieved 77-fs RMS jitter and –40-dBc IPN at 28.5 GHz. The phase noises at 3.8 and 28.5 GHz were measured in the blue line and the red line, respectively. Due to the wide injection bandwidth more than 200 MHz of the mmW-band ILFM, the phase noise of the mmW-band ILFM followed the phase noise of the SSPLL with the theoretical value, 20log(N_2). Figure 28 shows that the proposed mmW-band frequency synthesizer based on a digital SSPLL achieved 74-fs RMS jitter and–40-dBc IPN at 29.25 GHz. Figure 29 shows that the levels of the 100-MHz reference spur and the 1.9-GHz injection spur were −58 and −40 dBc, respectively.

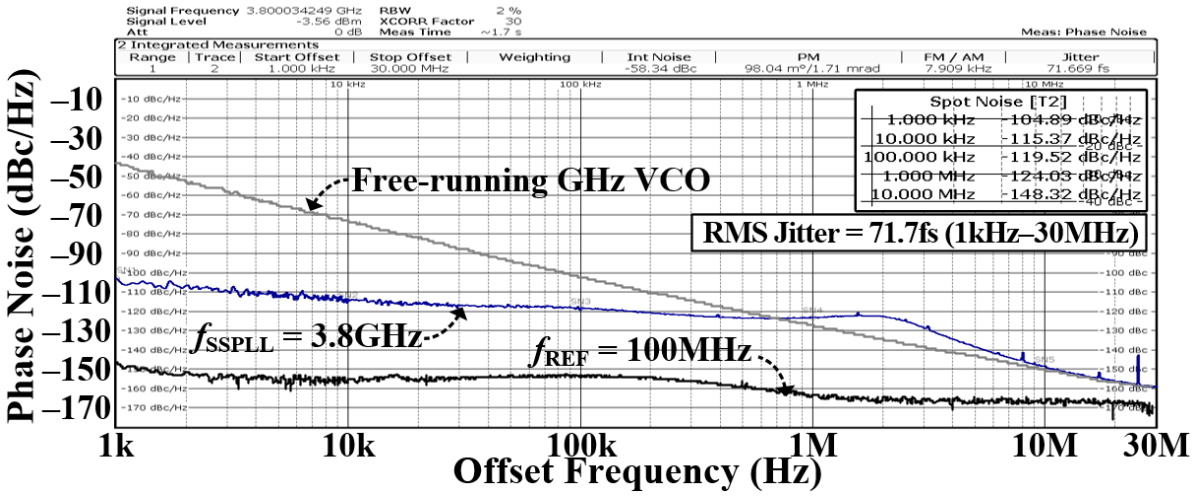


Figure 23. Measured phase noise at 3.8 GHz.

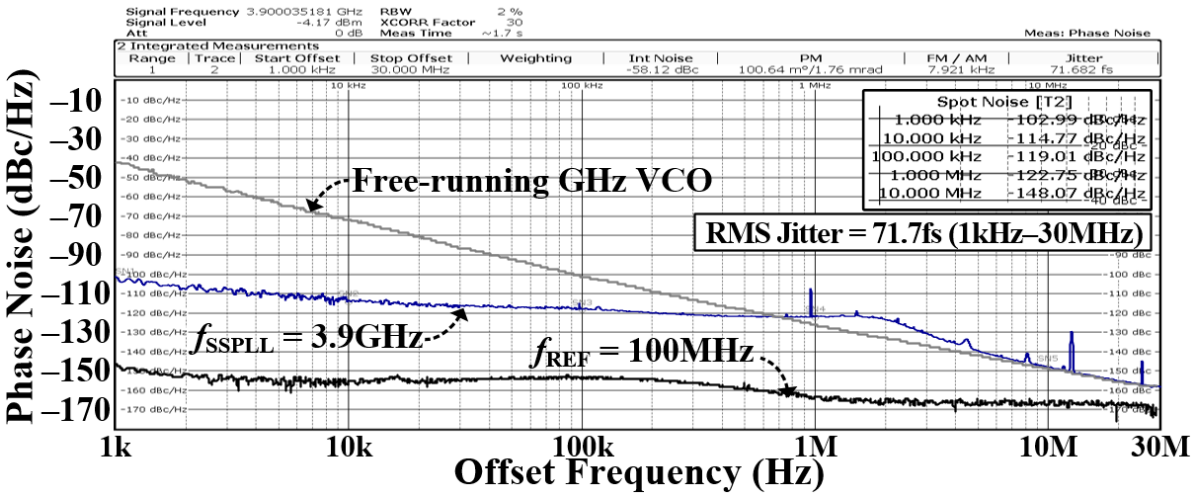


Figure 24. Measured phase noise at 3.9 GHz.

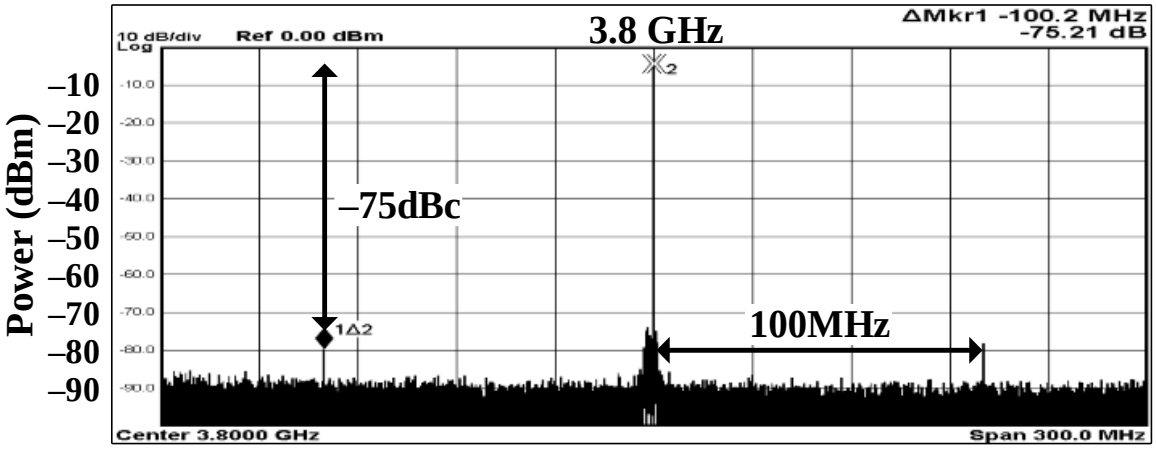


Figure 25. Measured spectrum at 3.8 GHz.

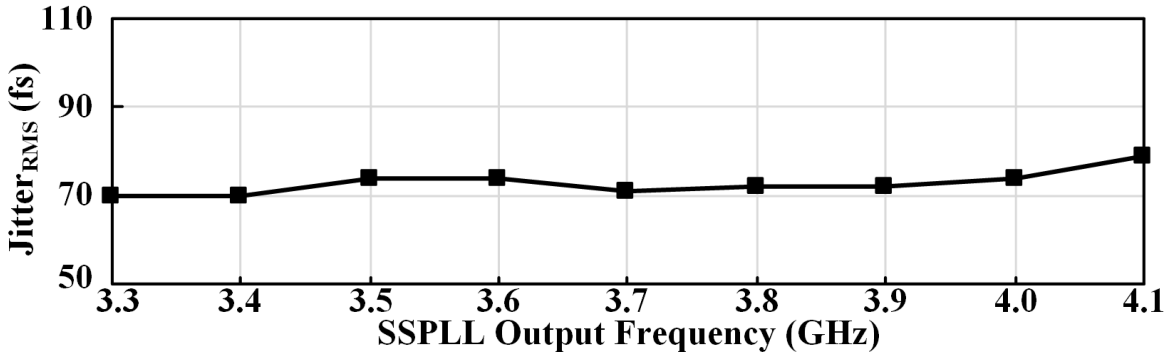


Figure 26. Variations in the RMS jitter over GHz frequencies.

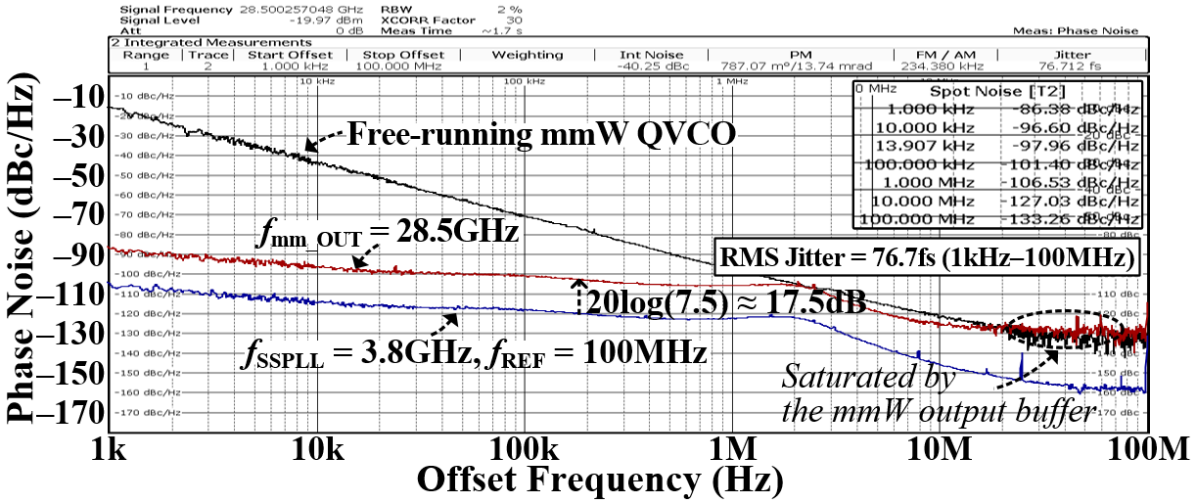


Figure 27. Measured phase noise at 28.5 GHz.

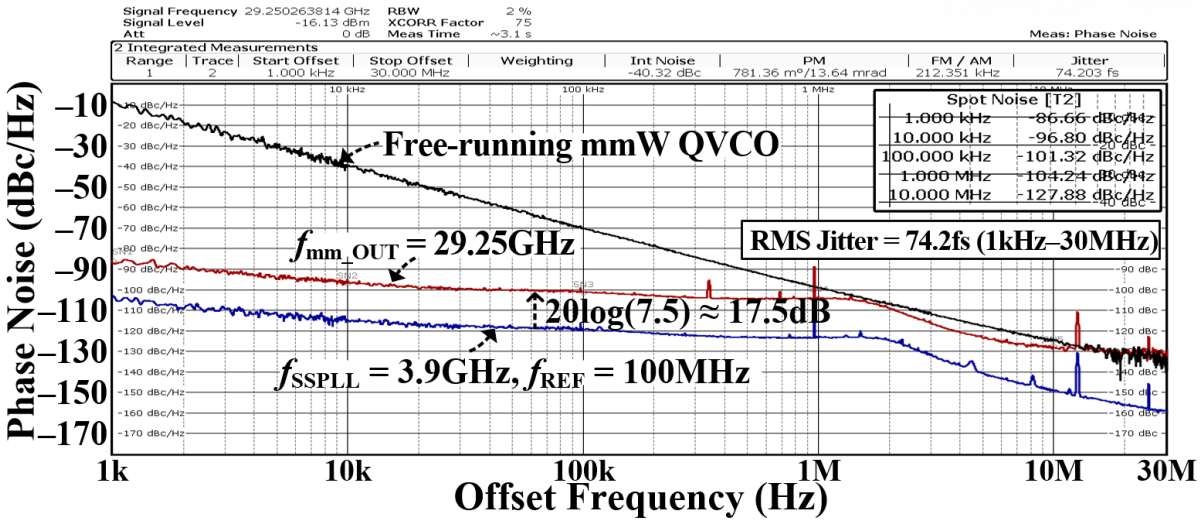


Figure 28. Measured phase noise at 29.25 GHz.

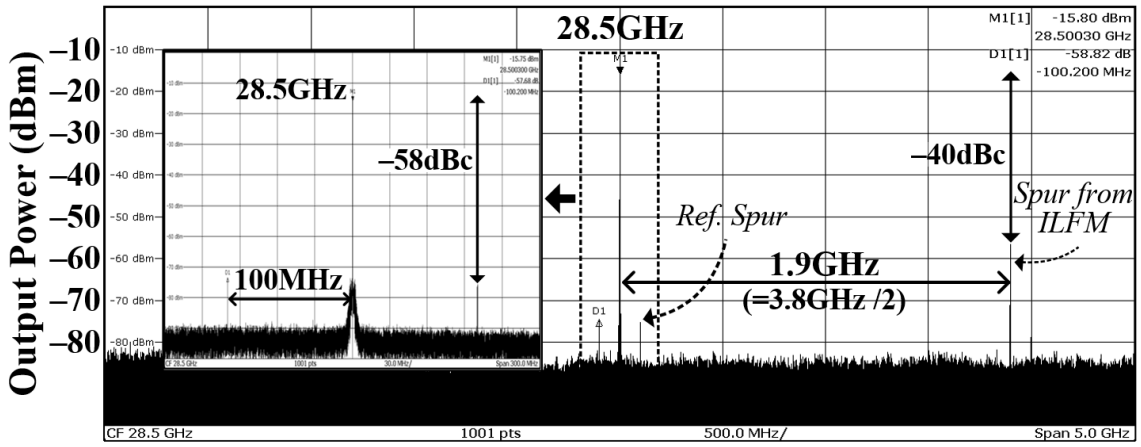


Figure 29. Measured spectrum at 28.5 GHz.

As shown in Table 2, the proposed digital SSPLL achieved the lowest RMS jitter of 72 fs and the FoM_{JIT} of −250 dB among GHz-band SSPLLs. Table 3 shows the comparison of the performance of the proposed cascaded frequency synthesizer with that of mmW-band frequency synthesizers. This work achieved the lowest RMS jitter of 77 fs and the lowest FoM_{JIT} of −250 dB among them. The FoMs of GHz-band SSPLLs and mmW-band frequency synthesizers are benchmarked in the left and the right of Fig. 30, respectively. Among all GHz-band SSPLLs, the proposed digital SSPLL achieved the lowest RMS jitter. Among all mmW-band frequency synthesizers, the proposed mmW-band frequency synthesizer achieved the lowest RMS jitter and the lowest FoM_{JIT}.

Table 2. Comparison with the state-of-the-art SSPLLs in GHz-band.

	This work	JSSC'18 [11]	ISSCC'15 [13]	JSSC'16 [14]	JSSC'18 [9]
Process	65nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	Digital SSPLL	Analog SSPLL	Digital SSPLL	Digital SSPLL	Analog SSPLL
Topology	OSVC-based	SS-PD based	ADC-based	ADC-based	SS-PD based
Type	Integer-*N*	Fractional-*N*	Fractional-*N*	Integer-*N*	Integer-*N*
f_{SSPLL} (GHz)	3.3–4.1	2.39–2.46	2.6–3.9	2.2	4.6–5.6
f_{REF} (MHz)	100	50	49.15	100	100
RMS jitter (fs) (Integ. Range)	72 (1 k–30 MHz)	169 (10 k–30 MHz)	226 (1 k–100 MHz)	380 (10 k–40 MHz)	162.2 (10 k–100 MHz)
Ref. spur (dBc)	–75 @3.8	–72 @2.397	–60 @2.68	–74 @2.2	–64 @5.0
Power (P_{DC}) (mW)	19.1	21.0	11.5	4.2	1.1
Active Area (mm^2)	0.21	0.43	0.23	0.15	0.01
FoM_{JIT} (dB)**	–250.1	–242.2	–242.3	–242.2	–255.4

Table 3. Comparison with the state-of-the-art frequency synthesizers in mmW-bands.

	This work	JSSC'15 [32]	ISSCC'17 [33]	ISSCC'18 [7]	JSSC'16 [34]
Process	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Architecture	Digital SSPLL + ILFM	60GHz SS QPLL	All-Digital PLL	RFD + CPPLL + ILFMs	20GHz SSPLL + 60GHz QILO
Type	Integer-*N*	Integer-*N*	Fractional-*N*	Fractional-*N*	Integer-*N*
Quadrature	YES	YES	NO	YES	YES
f_{OUT} (GHz)	28.0–31.0	53.8–63.3	50.2–66.5	25.0–30.0	55.6–65.2
f_{REF} (MHz)	100	40	100	120	40
RMS jitter (fs) (Integ. Range)	77 (1 k–100 MHz)	230 (1 k–100 MHz)	258 (1 k–40 MHz)	206 (1 k–100 MHz)	290 (10 k–40 MHz)
IPN (dBc) Norm. to 28 GHz (Integ. Range)	–40.3 (1 k–100 MHz)	–30.8 (1 k–100 MHz)	–29.9 (1 k–40 MHz)	–31.8 (1 k–100 MHz)	–28.8* (10 k–40 MHz)
In-band noise (dBc/Hz) Norm. to 28 GHz	–96.8	–88.1*	–86.1	–89.0	–85.2
Ref. spur (dBc)	–58	–40	NA	–83	–73
Power (P_{DC}) (mW)	41.8	42.0	46.0	36.4	32.0
Active Area (mm^2)	0.32	0.16	0.45	0.95	1.08 w/ pads
FoM_{JIT} (dB)**	–246.1	–236.5	–235.1	–238.1	–235.7

* Calculated from measurements ** $FoM_{JIT}=10\log(\sigma_t^2 \cdot P_{DC})$ dB

6. Conclusions

In this thesis, the frequency synthesizers based on a cascaded architecture were presented. First, the proposed mmW-band based on a CP PLL achieved an ultra-low IPN of –31 dBc. However, due to the poor performance of the in-band phase noise, it is hard to improve further. Meanwhile, by replacing the first stage with the proposed digital SSPLL, it achieved a very low in-band phase noise due to the the subsampling operation and the minimization of the quantization error of the proposed OSVC. Additionally, by using the GHz-band *LC* VCO having a high-quality factor, the out-band phase noise of the SSPLL was suppressed. The proposed OSVC reduced the quantization noise significantly while requiring ultra-low power consumption and small area due to the use of only three VCs. At the second stage, since the mmW-band ILFM had a very wide VCO-noise-suppression bandwidth, the noise contribution of the mmW-band signal was almost negligible. In measurement results, the proposed frequency synthesizer generated the mmW-band signals, which had the sub-80fs RMS jitter and the IPN of less than –40 dBc.

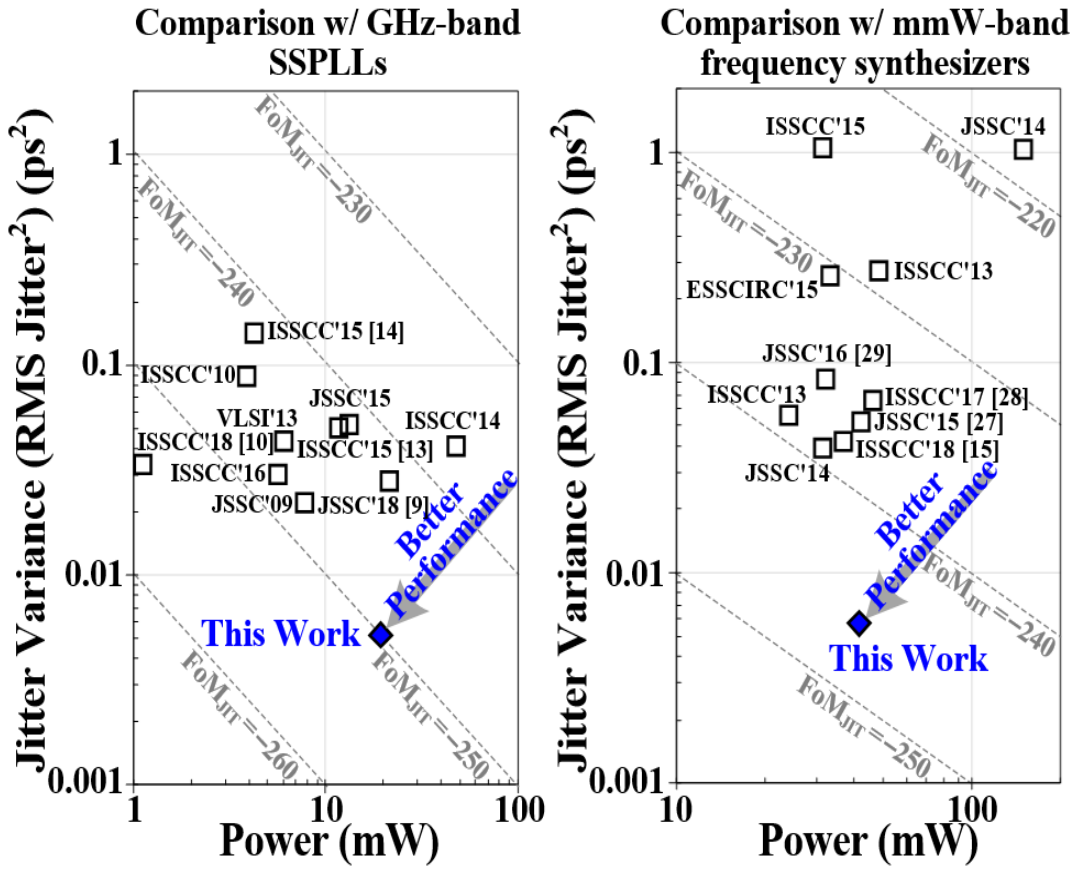


Figure 30. Benchmarking performance for GHz-SSPLLs and mmW-band frequency synthesizers.

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